ADITYA ENGINEERING COLLEGE

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Department of Electronics and Communication Engineering

M.Tech. (VLSI Design) - AR17 - Course Articulation Matrix

Note: Correlation Levels are 1 or 2 or 3. Where 1- Slight(Low), 2 - Moderate(Medium), 3 - Substantial (High).

	CO Statements	POs											PSOs		
I SEM															
Course Code	**172EM1T01-DIGITAL SYSTEM DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Examine CAMP Algorithms for minimizing the complexity of digital system design.	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
CO2	Simplify digital circuits using PLA minimization algorithm (IISc algorithm) and PLA folding algorithm	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**
CO3	construct digital circuits using CPLDs, FPGAs and ASICs	**1**	**2**	**1**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**-**
CO4	Analyze the functionality of combinational circuits using different fault diagnosis & test methods.	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**-**
CO5	Analyze the testing aspects and fault diagnosis methods of sequential circuits.	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**-**
Course Code	**172VD1T01-VLSI TECHNOLOGY AND DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Summarize the fundamental concepts of VLSI technology including both fabrication process and basic design elements.	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**2**	**1**	**1**
CO2	Analyze the various VLSI design technologies and design issues.	**-**	**3**	**2**	**-**	**2**	**-**	**-**	**-**	**2**	**-**	**3**	**3**	**3**	**1**
CO3	Analyze the electrical properties, basic circuit concepts and scaling of the MOS devices.	**2**	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**3**	**1**
CO4	Develop a subsystem design process for VLSI circuits.	**1**	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**3**
CO5	Choose various floor planning methods for architecture design.	**-**	**-**	**-**	**3**	**2**	**-**	**-**	**3**	**2**	**-**	**1**	**2**	**3**	**2**
CO6	Identify various design methodologies for chip design.	**-**	**-**	**-**	**-**	**3**	**2**	**1**	**-**	**2**	**-**	**-**	**3**	**2**	**1**

	CO Statements	POs											PSOs		
Course Code	**172VD1T02-CMOS ANALOG IC DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Demonstrate the small signal and large signal models of CMOS transistors in different frequencies.	**1**	**1**	**-**	**2**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**2**	**1**	**-**
CO2	Analyze the characteristics of different CMOS circuits.	**1**	**3**	**2**	**2**	**-**	**-**	**1**	**-**	**-**	**-**	**-**	**3**	**3**	**1**
CO3	Develop the two stage CMOS operational amplifiers.	**1**	**2**	**-**	**3**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**3**	**3**	**1**
CO4	Analyze different comparators and their performance parameters.	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**3**
CO5	Develop the basic circuits based on the knowledge acquired in the course.	**1**	**2**	**1**	**-**	**3**	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**2**	**-**
Course Code	**172VD1T03-CMOS DIGITAL IC DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain the functionality of MOS inverters	**-**	**1**	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**-**
CO2	Analyze various combinational circuits designs in CMOS	**2**	**3**	**2**	**-**	**3**	**3**	**-**	**3**	**-**	**-**	**-**	**3**	**3**	**-**
CO3	Analyze sequential logic gates designs in CMOS	**2**	**3**	**2**	**-**	**3**	**3**	**-**	**3**	**-**	**-**	**-**	**3**	**3**	**-**
CO4	Explain the functionality of different arithmetic building blocks	**-**	**1**	**-**	**-**	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**2**	**1**	**-**
CO5	Analyze different semiconductor memories	**2**	**3**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**3**	**3**	**1**
Course Code	**172EM1E01-CYBER SECURITY (ELECTIVE - I)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Discover the various security attacks and security services	**2**	**3**	**2**	**3**	**3**	**3**	**-**	**-**	**3**	**3**	**3**	**3**	**-**	**-**
CO2	Develop a model for Internetwork security	**1**	**2**	**1**	**3**	**3**	**2**	**-**	**3**	**3**	**3**	**2**	**-**	**2**	**-**
CO3	Analyze threats and risks within context of the cyber security architecture	**-**	**3**	**2**	**-**	**-**	**3**	**-**	**-**	**3**	**3**	**3**	**3**	**-**	**-**
CO4	Utilize cryptography algorithms, digital signatures, digital Certificates and Key Management	**1**	**-**	**2**	**3**	**3**	**3**	**-**	**-**	**3**	**-**	**2**	**3**	**-**	**-**
CO5	Interpret the IP Security and its implementation of architecture, SSL, TLS	**3**	**3**	**3**	**3**	**3**	**3**	**-**	**3**	**3**	**3**	**3**	**3**	**-**	**2**

	CO Statements	POs											PSOs		
CO6	Make use of the intrusion detection system and Firewall	**1**	**2**	**1**	**3**	**3**	**2**	**-**	**-**	**3**	**3**	**2**	**3**	**-**	**-**
Course Code	**172VD1E01-DIGITAL DESIGN USING HDL (ELECTIVE - I)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Interpret the HDL design styles, data types to implement the basic digital circuits.	**-**	**1**	**-**	**-**	**2**	**-**	**-**	**3**	**-**	**-**	**-**	**2**	**1**	**-**
CO2	Analyze the basic logic circuits in Xilinx tool.	**-**	**-**	**2**	**-**	**3**	**3**	**-**	**-**	**3**	**-**	**-**	**3**	**3**	**1**
CO3	Apply the HDL knowledge to implement combinational and sequential digital circuits.	**-**	**2**	**-**	**-**	**3**	**-**	**-**	**-**	**3**	**-**	**-**	**3**	**2**	**-**
CO4	Make use of the Xilinx tool Knowledge to synthesis the combinational and sequential circuits.	**-**	**2**	**-**	**-**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**-**
CO5	Test for the functionality of digital circuit by using various fault models	**-**	**-**	**-**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**1**
Course Code	**172CO1E02-ADVANCED OPERATING SYSTEMS (ELECTIVE - I)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain the basic concept of operating systems.	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO2	Interpret the high-level structure of the Unix and Linux kernels.	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**-**	**-**
CO3	Analyze the concepts of processes, resource control, physical and virtual memory, scheduling, I/O and files.	**2**	**-**	**2**	**3**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**-**
CO4	Illustrate the concept of distributed operating systems.	**-**	**1**	**-**	**-**	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**-**
CO5	Develop the Mutual exclusion, Deadlock detection and agreement protocols.	**1**	**-**	**-**	**-**	**3**	**2**	**-**	**-**	**3**	**3**	**-**	**3**	**2**	**-**
Course Code	**172EM1E03-SOFT COMPUTING TECHNIQUES (ELECTIVE - I)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Describe the soft computing techniques and their roles in building intelligent machines.	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**-**
CO2	Apply the Artificial Neural Networks knowledge for solving the linear problems.	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO3	Apply the fuzzy logic and reasoning knowledge for solving the uncertainty in engineering problems.	**-**	**2**	**-**	**2**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
CO4	Apply genetic algorithms to combinatorial optimization problems.	**-**	**2**	**-**	**2**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**

	CO Statements	POs											PSOs		
CO5	Compare solutions by various soft computing approaches for a given problem.	**-**	**3**	**3**	**3**	**3**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**
Course Code	**172EM2T08-CPLD/FPGA ARCHITECTURES & APPLICATIONS (ELECTIVE - II)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Identify different types of programmable logic devices.	**1**	**-**	**1**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO2	Compare the performance of different FPGAs and their programming Technologies.	**-**	**-**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO3	Analyze different SRAM programmable FPGA architectures.	**2**	**3**	**2**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**-**
CO4	Analyze different Anti-Fuse Programmed FPGA architectures.	**2**	**3**	**2**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**-**
CO5	Develop digital circuits with ACT architectures.	**1**	**2**	**1**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**3**
Course Code	**172VD1E03-HARDWARE SOFTWARE CO-DESIGN (ELECTIVE - II)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Analyze embedded system’s hardware and software design issues.	**2**	**3**	**-**	**3**	**3**	**-**	**1**	**-**	**-**	**-**	**-**	**3**	**3**	**1**
CO2	Analyze embedded system’s hardware and software design issues.	**-**	**2**	**1**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**2**	**-**
CO3	Demonstrate modern embedded architectures and compilation technologies.	**-**	**1**	**-**	**2**	**2**	**-**	**-**	**3**	**-**	**-**	**-**	**3**	**2**	**1**
CO4	Interpret the Design, co design by using design verification tools.	**-**	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**3**	**-**	**1**	**2**	**1**	**-**
CO5	Build the system from system level specification languages.	**-**	**2**	**1**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**1**
Course Code	**172EM1E07-ADVANCED COMPUTER ARCHITECTURE (ELECTIVE - II)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Compare the performance of different computer architectures with respect to changing faces of computing and Technology trends.	**2**	**-**	**2**	**3**	**-**	**-**	**1**	**-**	**-**	**-**	**3**	**3**	**3**	**1**
CO2	Examine the operation of modern CPUs including pipelining and memory systems.	**2**	**3**	**2**	**-**	**3**	**-**	**1**	**-**	**-**	**-**	**-**	**3**	**3**	**1**
CO3	Explain instruction level parallelism with dynamic scheduling, Static branch prediction and VLIW approach.	**-**	**1**	**-**	**2**	**2**	**1**	**-**	**3**	**-**	**-**	**1**	**2**	**1**	**-**
CO4	Identify the best multi processors with respect to Thread level Parallelism, Memory architecture and Synchronization.	**1**	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**	**-**

	CO Statements	POs											PSOs		
CO5	Measure the Practical issues in the interconnecting networks	**-**	**3**	**3**	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**2**
Course Code	**172VD1L01-FRONT END VLSI DESIGN - LAB**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Develop VHDL code for basic combinational and sequential digital modules.	**1**	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**3**	**-**	**2**	**1**	**1**	**2**
CO2	Test for functional verification of digital circuits with the aid of I-Sim simulator.	**1**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**
CO3	Inspect the VHDL code under given user constraints using CAD tools.	**2**	**-**	**2**	**2**	**3**	**-**	**1**	**3**	**2**	**-**	**-**	**2**	**2**	**3**
CO4	Analyse the synthesize report in order to meet the given constraints.	**2**	**3**	**-**	**2**	**3**	**-**	**1**	**3**	**2**	**-**	**3**	**2**	**2**	**3**
CO5	Utilize the FPGA and CPLD devices for real time verification.	**1**	**-**	**1**	**3**	**2**	**1**	**1**	**2**	**-**	**-**	**-**	**1**	**1**	**2**
II SEM															
Course Code	**172VD2T04-CMOS MIXED SIGNAL CIRCUIT DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Apply the knowledge of basic sciences and engineering to design CMOS analog and digital circuits.	**1**	**2**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**3**
CO2	Analyze the concepts of basic topology in Phase locked loops	**2**	**3**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**3**
CO3	Illustrate the fundamentals of different types of data converters.	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO4	Design flash converters, successive approximation type and pipelined converters.	**-**	**-**	**-**	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**3**	**3**
CO5	Analyze delta sigma modulators, noise shaping data converting circuits using filters.	**2**	**3**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**3**
Course Code	**172VD2T05-EMBEDDED SYSTEM DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Describe the differences between the general computing system and the embedded system.	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**2**
CO2	Analyze the hardware components, processor performance of an embedded system design.	**2**	**3**	**2**	**-**	**-**	**3**	**-**	**-**	**3**	**-**	**-**	**3**	**3**	**1**
CO3	Make use of operating systems and embedded programming languages to develop a real-time system.	**1**	**2**	**1**	**3**	**3**	**2**	**-**	**-**	**3**	**-**	**-**	**3**	**2**	**-**

	CO Statements	POs											PSOs		
CO4	Utilize modern development tools, CAD tools for integrating software and hardware components in embedded system designs.	**1**	**2**	**1**	**3**	**3**	**2**	**-**	**-**	**3**	**-**	**-**	**3**	**2**	**-**
CO5	Design an embedded system by understanding the various processor architectures case studies along with its applications.	**1**	**2**	**1**	**3**	**3**	**2**	**-**	**-**	**3**	**-**	**-**	**3**	**3**	**3**
Course Code	**172VD2T06-LOW POWER VLSI DESIGN**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits.		**1**	**-**	**-**	**2**	**-**	**-**	**-**	**-**	**-**	**1**	**-**	**-**	**1**
CO2	Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.	**1**	**2**	**-**	**3**	**-**	**2**	**-**	**-**	**-**	**3**	**-**	**1**	**1**	**3**
CO3	Compare the different low power VLSI Design techniques that are available to design an Integrated Circuit for commercial applications	**-**	**-**	**1**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**3**
CO4	Analyze CMOS circuit by knowing the characteristics of various CMOS technologies and processes.	**2**	**3**	**-**	**3**	**3**	**-**	**1**	**-**	**-**	**-**	**3**	**2**	**2**	**3**
CO5	Develop a VLSI project having a set of objective criteria and design constraints.	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**2**	**3**	**2**	**-**
Course Code	**172VD2T07-DESIGN FOR TESTABILITY**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Apply the fundamental concepts of Testing in VLSI design.	**1**	**2**	**1**	**3**	**-**	**2**	**-**	**-**	**3**	**-**	**2**	**3**	**2**	**-**
CO2	Apply simulation algorithms for verification and validation.	**1**	**2**	**1**	**-**	**3**	**2**	**-**	**-**	**3**	**-**	**2**	**3**	**4**	**-**
CO3	Evaluate a digital system using Testability Measures.	**-**	**-**	**3**	**-**	**-**	**3**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**1**
CO4	Develop skills in the modelling of BIST Architecture and Memory BIST.	**-**	**2**	**1**	**-**	**3**	**2**	**-**	**-**	**-**	**3**	**-**	**3**	**2**	**-**
CO5	Assess logic and technology-septic parameters in Boundary Scan Standards	**-**	**-**	**3**	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**3**	**3**	**-**	**2**
Course Code	**172VD2E04-CAD FOR VLSI (ELECTIVE - III)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain the VLSI physical Design automation	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**-**	**-**	**2**	**-**	**-**
CO2	Apply Algorithms Required for partitioning, floor planning, pin assignment placement	**1**	**2**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**2**	**-**

	CO Statements	POs											PSOs		
CO3	Explain global and detailed routing	-	1	-	-	-	-	-	3	3	-	-	2	1	-
CO4	Demonstrate Physical design automation of FPGAs and MCMs.	-	1	-	-	-	-	-	3	3	-	-	2	-	-
CO5	Analyze the Chip input and output circuits to protect against ESD	2	3	-	-	-	-	-	3	3	-	-	3	3	1
Course Code	**172EM2T06-DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (ELECTIVE - III)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Demonstrate various issues that are needed in implementing DSP algorithms under given constraints.	1	2	-	3	-	-	-	3	-	-	-	-	1	2
CO2	Interpret the various modules involved in a DSP system	-	1	-	-	2	-	-	3	-	-	-	-	-	2
CO3	Apply the concepts of Interrupts and on-chip peripherals in programming	-	-	-	-	-	-	-	-	-	-	-	2	-	3
CO4	Analyze different architecture details and instruction sets of fixed, floating point DSPs.	2	3	-	3	-	-	2	-	-	-	2	2	2	3
CO5	Perceive the interfacing of DSP devices with various modules such as DMA, parallel I/O interface.	-	-	3	3	-	-	3	3	-	-	3	-	2	3
Course Code	**172VD2E05-VLSI SIGNAL PROCESSING (ELECTIVE - III)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain parallel and pipelining processing techniques.	2	3	3	-	3	3	-	3	-	-	-	2	-	-
CO2	Identify applications for unfolding algorithm	3	1	-	-	2	-	-	-	-	-	-	3	-	-
CO3	Analyse Systolic Design for Space Representations containing Delays	3	3	2	-	-	-	-	-	-	-	-	3	-	-
CO4	Explain Cook-Toom Algorithm, Fast Convolution algorithm by Inspection method.	2	1	1	-	2	-	-	-	-	-	-	2	-	-
CO5	Analyze Power Reduction techniques and Power Estimation techniques	3	3	2	-	-	-	-	3	-	-	-	4	-	1
Course Code	**172EM2E08-SYSTEM ON CHIP DESIGN (ELECTIVE - IV)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Explain all the building blocks of System-on-Chip.	-	-	-	2	-	1	-	-	3	-	-	2	-	-
CO2	Classify the concept of processors and instruction handling.	-	-	-	2	-	1	-	-	3	-	-	2	-	-
CO3	Analyze vector, VLIW and superscalar processors.	2	3	2	3	-	3	1	3	3	-	3	3	-	1
CO4	Design a Memory as part of System-on-Chip.	1	2	1	3	-	2	-	3	-	-	2	3	2	-

	CO Statements	POs											PSOs		
CO5	Illustrate the concepts of interconnect optimization and configuration in System-on-Chip.	-	-	-	2	-	1	-	-	3	-	-	2	-	-
Course Code	**172VD2E06-OPTIMIZATION TECHNIQUES IN VLSI DESIGN (ELECTIVE - IV)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Compare various statistical modelling methods such as Monte carlo techniques, Pelgroms methods, principle component based and quad tree based modelling methods.	-	1	-	2	2	-	-	-	-	-	-	-	-	-
CO2	Analyze the systems by using concepts of high level and gate level statistical methods.	2	3	2	3	-	-	-	-	-	-	-	3	3	2
CO3	Explain the concepts of geometric programming and convex functions.	-	1	-	2	2	-	-	-	-	-	-	-	-	-
CO4	Develop the real time applications using optimization techniques such as Genetic Algorithms.	-	-	-	3	-	2	-	-	-	-	-	3	-	-
CO5	Apply CMOS technology -specific layout rules in the placement and routing of transistor sand to verify the functionality, timing and power	1	2	-	3	3	-	-	-	-	-	-	3	2	-
Course Code	**172VD2E07-SEMICONDUCTOR MEMORY DESIGN AND TESTING (ELECTIVE - IV)**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Analyze the different RAM architectures and interconnects.	2	3	-	3	-	-	-	-	-	-	-	3	-	1
CO2	Classify High-Performance Subsystem Memories.	2	3	-	3	-	-	-	-	-	-	-	3	-	1
CO3	Explain different fault modeling and testing techniques.	-	-	-	2	-	-	-	-	-	-	-	2	-	-
CO4	Develop reliable memory architectures by considering radiation affects.	1	2	-	3	-	-	-	-	-	-	-	3	-	-
CO5	Identify new developments in semiconductor memory design	1	2	-	3	-	-	-	-	-	-	-	2	-	-
Course Code	**172VD2L02-BACK END VLSI DESIGN LAB**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	Identify different HDL description styles for various logic designs.	-	2	1	3	-	-	-	-	-	-	-	1	1	3
CO2	Compare schematics for all digital designs and implement using simulation tools.	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO3	Discover layouts physically through various Back end EDA Tools	-	-	2	3	3	3	-	-	3	-	-	2	2	3
CO4	Examine the performance extracted layouts through DRC,LVS, and PEX	3	-	-	-	-	-	-	-	3	3	3	3	3	3
CO5	Evaluate the performance of combinational and sequential designs for its speed and other performance parameters	3	3	3	3	-	3	2	-	-	-	-	3	3	3